

September 1997 - Revised May 2000

High Speed CMOS Logic Quad 2-Input OR Gate

Features

- **Typical Propagation Delay:** 7ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^{\circ}C$
- **Fanout (Over Temperature Range)**
 - **Standard Outputs** **10 LSTTL Loads**
 - **Bus Driver Outputs** **15 LSTTL Loads**
- **Wide Operating Temperature Range** . . . **$-55^{\circ}C$ to $125^{\circ}C$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
 - **2V to 6V Operation**
 - **High Noise Immunity:** $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- **HCT Types**
 - **4.5V to 5.5V Operation**
 - **Direct LSTTL Input Logic Compatibility,** $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - **CMOS Input Compatibility,** $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC32 and 'HCT32 contain four 2-input OR gates in one package. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

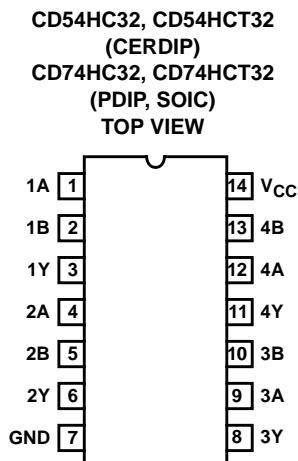
Ordering Information

PART NUMBER	TEMP. RANGE ($^{\circ}C$)	PACKAGE
CD54HC32F3A	-55 to 125	14 Ld CERDIP
CD54HC32W	-55 to 125	Wafer
CD74HC32E	-55 to 125	14 Ld PDIP
CD74HC32M	-55 to 125	14 Ld SOIC
CD54HCT32F	-55 to 125	14 Ld CERDIP
CD54HCT32F3A	-55 to 125	14 Ld CERDIP
CD74HCT32E	-55 to 125	14 Ld PDIP
CD74HCT32M	-55 to 125	14 Ld SOIC

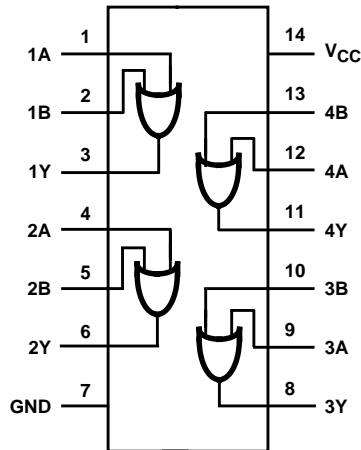
NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinout



Functional Diagram

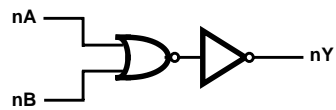


TRUTH TABLE

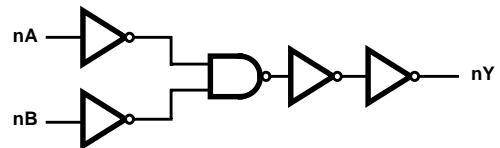
INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

NOTE: H = High Voltage Level, L = Low Voltage Level

HC Logic Symbol



HCT Logic Symbol



CD54/74HC32, CD54/74HCT32

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}\text{C/W}$)	θ_{JC} ($^{\circ}\text{C/W}$)
PDIP Package	100	N/A
CERDIP Package	130	55
SOIC Package	180	N/A
Maximum Junction Temperature (Hermetic Package or Die) . . .	175 $^{\circ}\text{C}$	
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}\text{C}$	
Maximum Storage Temperature Range	-65 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$	
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}\text{C}$	
(SOIC - Lead Tips Only)		

Operating Conditions

Temperature Range (T_A)	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	.2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	2	-	20	-	40	μA

CD54/74HC32, CD54/74HCT32

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	-0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	-	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	2	-	20	-	40	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	1.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Input to Output (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	90	-	115	-	135	ns
			4.5	-	-	18	-	23	-	27	ns
			6	-	-	15	-	20	-	23	ns
Propagation Delay, Data Input to Output Y	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	7	-	-	-	-	-	ns
Transition Times (Figure 1)	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns

CD54/74HC32, CD54/74HCT32

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	22	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, Input to Output (Figure 2)	t_{RHL}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	24	-	30	-	36	ns
Propagation Delay, Data Input to Output Y	t_{PLH}, t_{PLH}	$C_L = 15\text{pF}$	5	-	9	-	-	-	-	-	ns
Transition Times (Figure 2)	t_{TLH}, t_{TLH}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	22	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

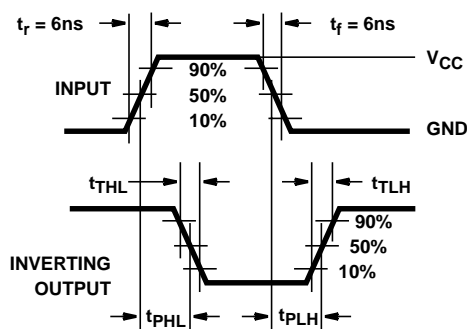


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

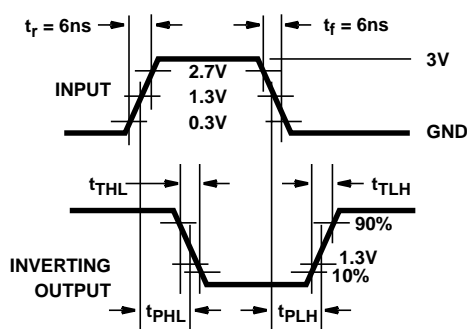


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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